Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A method for forming a memory device, comprising:

providing a stacked structure on a substrate, the stacked structure comprising a first dielectric, a floating gate, a second dielectric, and a control gate;

forming a liner dielectric layer ~~that~~, which extends in a direction transverse to a bit line direction and substantially parallel to the control gate, on sidewalls of the stacked structure; and

forming a barrier layer on at least part of the liner dielectric layer.

2. (Original) The method as set forth in claim 1, wherein the providing of a stacked structure on a substrate comprises:

forming a first dielectric layer on the substrate;

forming a floating gate on the first dielectric layer;

forming a second dielectric layer on the floating gate; and

forming a control gate on the second dielectric layer.

3. (Original) The method as set forth in claim 1, wherein the forming of a barrier layer comprises forming a silicon nitride layer.

4. (Original) The method as set forth in claim 3, wherein:

the memory device comprises at least one flash memory cell;

the method comprises implanting dopants into areas of the substrate to form source and drain regions within the substrate; and

the method further comprises forming a silicon dioxide spacer on the silicon nitride layer.

5. (Original) The method as set forth in claim 3, wherein the forming of the liner dielectric layer comprises performing thermal oxidation such that the liner dielectric layer comprises silicon dioxide.

6. (Original) The method as set forth in claim 5, wherein the forming of the silicon nitride layer comprises chemical vapor deposition (CVD) of silicon nitride.

7. (Original) The method as set forth in claim 6, wherein a thickness of the silicon nitride layer is larger than about 30 Å.

8. (Original) The method as set forth in claim 5, wherein the forming of the silicon nitride layer comprises performing a nitridation process.

9. (Original) The method as set forth in claim 8, wherein the performing of a nitridation process comprises performing rapid thermal processing in the presence of NO, N2 , N2O or NH32O.

10. (Original) The method as set forth in claim 9, wherein the forming of the silicon nitride layer comprises forming the silicon nitride layer to a thickness greater than about 10 Å.

11. (Original) The method as set forth in claim 8, wherein the forming of the silicon nitride layer comprises exposing the liner dielectric layer to an N2 plasma.

12. (Original) The method as set forth in claim 11, wherein the forming of the silicon nitride layer comprises forming the silicon nitride layer to a thickness greater than about 10 Å.

13. (Original) The method as set forth in claim 1, wherein the providing comprises providing a stacked structure comprising a second dielectric, which includes:

a lower layer of insulator material;

a middle layer of charge trapping material formed on the lower layer; and

an upper layer of insulator material formed on the middle layer.

14. (Original) The method as set forth in claim 1, wherein the providing comprises providing a stacked structure comprising a second dielectric, which includes:

a lower layer of oxide;

a middle layer of nitride formed on the lower layer; and

an upper layer of oxide formed on the middle layer.

15. (Original) The method as set forth in claim 1, wherein the liner dielectric and the barrier layer are formed to extend over source/drain regions of the memory device.

16. (Original) The method as set forth in claim 1, wherein the liner dielectric and the barrier layer are formed not to extend over source/drain regions of the memory device.

17-31. (Cancelled)